REMARKS/ARGUMENTS

Claim Rejections - 35 USC § 103

"Claims 10-11, 22-23 remain rejected under 35 U.S.C 102(3) as being unpatentable over Flannagan (U.S Patent No. 6,031,408) and further in view of Li (U.S Patent No. 6,836,160) for the reasons recited in the last Office action".

Applicants submit there is no suggestion or incentive to combine Flannagan and Li. Li is a current generator circuit to source a fairly constant current with a temperature dependency requiring bipolar transistors (bipolar only in order to generate the correct temperature dependency) and emitter resistors divider; whereas Flanagan is a MOSFET clamp circuit with no temperature dependency and the current is normally shut off unless the voltage at a node exceed some limit. Further, Flannagan Col 12 L 31-38 states "such a mirroring technique can be used, along with the sizing of the transistors 132 and 136 ... for optimum performance." Thus, Flannagan states he achieves his optimum performance by resizing his transistors, and not by adding any additional components. Since Flannagan can already achieve optimum performance, there is no incentive to combine another element such as from Li. Yet further, the three goals of Flannagan's circuit (Col 12 L 43-55) indicate there is no desirability nor suggestion to modify his circuit in the manner of Li who has goals completely unrelated to Flannagan's; Flannagan would not look to Li.

Therefore, Claims 10 and 22 (currently amended) should be patentable over Flannagan in view of Li.

Claims 10-11 and 22-23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Beeman (U.S Patent No. 6,614,284).

Applicants traverse the rejection based on Beeman. First, Beeman does not teach the "biasing circuit" recited in Claim 10 and the "clamping circuit ensuring that a voltage level at a node is within a specified range" recited in Claim 22; instead, Beeman has an emitter follower circuit (Col 1 L6-10) that transfers a signal to the base of Q21, not to the source of Q21, without ever clamping it. Second, Beeman's circuit topology does not match the recitation. Beeman Fig. 5 does not anticipate "a source terminal of said third transistor is connected to ground" as recited in Claims 10 and 22. In contrast, Beeman has a resistor between the source terminal and ground for his third transistor (Q23). And it is not clear whether the Examiner intended to refer to Fig. 2 instead of 1 of Beeman; in any case, neither Fig. 1 nor 2 anticipates the circuit topology and resistor as recited in Claims 10 and 22. Third, the operation does not match. Claims 10 and 22, as amended, recite "a first transistor with a source terminal connected to said node designed to be turned on when said voltage level is outside of said specified range". In contrast, Beeman's first transistor Q21 is turned on by Vin at the base of Q21 (Fig. 5). Q21's source is an output node N23; Q21 is not turned on by a voltage at the output node N23.
Therefore, Claims 10 and 22 (currently amended) should be patentable over Beeman.

Claims 10-11, 22 and 23 were also rejected under 35 U.S.C. 103(a) as being unpatentable over Flannagan (U.S Patent No. 6,031,408) and further in view of Kimura (U.S. Patent No. 5,990,727).

Applicants traverse the rejection of Claims 10 and 22 in light of the foregoing statements regarding the Flannagan reference (e.g. Flannagan achieves his optimum performance by resizing his transistors and thus there is no incentive to further combine a needless element from Kimura). Further, there is no incentive nor suggestion to combine Kimura with Flannagan, as Kimura's circuit provides an inverse PTAT current generator (Col 5 L 4-8, Col 8 L 25) and neither

Flannagan nor Applicants desire a circuit with a current having a negative temperature coefficient. Yet further, Kimura's resistor motivates away from Applicants circuit; Kimura's resistor exists solely to provide an inverse PTAT current (equation 5, Col 7 L36-42, Col 7 L55-60, Col 8 23-26, Col 9 14-20), an inverse proportional-to-temperature constant current (Col 7 L56, Col 9 L16). In contrast, Applicants clamp circuit is suppose to provide NO current unless the voltage at a node is out of range; it is a current non-linearly responsive to voltage and no particular temperature dependency. Whereas, Kimura desires a current linearly responsive to temperature.

Yet further, Applicants do not desire higher resistance and impedance as alleged by the Examiner on pages 5 and 6 of the Office Action. Instead, pages 29 – 30 of the disclosure indicate that the reason for the resistor allows for a smaller output transistor 1130, thus decreasing parasitics. As noted on page 46, some of the invention's applications are for wireless basestations and ADC's, where distortion is well known to be very important (ADC's are characterized by its THD, total harmonic distortion). Lower parasitics at the clamped node enable lower distortion and higher speed. Thus there is no incentive for Applicants to look to Flannagan or Kimura who have circuits which are not optimized for speed and distortion.

Therefore, Claims 10 and 22 (currently amended) should be patentable over Flannagan in view of Kimura.

Claims 11 and 23 being dependent on Claims 10 and 22, respectively, are believed allowable for the at least same foregoing reasons. Further, Applicants traverse the statement that FETs are "patentable equivalent to bipolar transistors since no unobvious results are seen produce from their use". In the reference the Examiner cited, there are discussions regarding the important differences leading Flannagan to invent a MOSFET (square-law) clamp circuit over a bipolar clamp circuit although both kinds of transistors are available to him in his

technology (see Fig. 4 and Col 1 L 52-67 and Col 2). However, Flannagan does not teach nor suggest the resistor. Therefore, Claims 11 and 23 which recite "NMOS transistors" with a clamp circuit containing a resistor are not obvious.

Allowable Subject Matter

Applicants thank the Examiner for allowing Claims 6-7 and 18-19.

New Claims

New Claims 26 and 27 being dependent on Claims 10 and 22, respectively, are believed allowable for the at least same foregoing reasons. Also, the cited references do not teach an ADC. Support for the new claims is found on p. 48 and Fig. 24 of the disclosure.

Respectful request is made for reconsideration of the application, as amended, and for an issuance of a Notice of Allowance.

Respectfully submitted,

/Dolly Y. Wu/
Dolly Y. Wu
Reg. No. 59,192
Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, Texas 75265
972.917.4144